CLAIMS

What is claimed is:

1   1.   A computer system that comprises:

2   an expansion bus that includes a plurality of expansion bus signals;

3   a bus bridge coupled to the expansion bus; and

4   a signal gate configurable to isolate the bus bridge from one of the expansion bus signals.

1   2.   The computer system of claim 1, further comprising:

2   a controller configured to receive said one of the expansion bus signals and configured to

3   determine whether said one of the expansion bus signals is driven in a non-standard

4   manner, wherein the controller sets the signal gate to isolate the bus bridge from the

5   expansion bus signal if the controller determines that the expansion bus signal is

6   driven in a non-standard manner.

1   3.   The computer system of claim 2, wherein said one of the expansion bus signals is a wake-

2   up signal.

1   4.   The computer system of claim 2, wherein said bus bridge is the south bridge.

1   5.   The computer system of claim 2, wherein said one of the expansion bus signals is a power

2   management event (PME#) signal, and wherein said controller determines that the PME# signal is

3   driven in a non-standard manner if the PME# signal is determined to be low at a predetermined

4   time delay after a Power Good signal goes low.

1   6.   The computer system of claim 2, wherein the controller is a power management controller.

1   7.   A computer system that comprises:

2   a user input device;

3   a computer chassis that contains at least:

4   a system memory configured to store an operating system;

5   a central processor coupled to the memory and configured to execute the operating

6   system;

7   an expansion bus that couples the user input device to the central processor;

8   a bus bridge coupled to the expansion bus, wherein the bus bridge includes:

9   a power management controller coupled to the expansion bus and

10   configured to receive a wake-up signal from a device resident on the

11   expansion bus, wherein the power management controller isolates

12   the wake-up signal from the bus bridge device if the device drives

13   the wake-up signal in a non-compliant manner.

1   8.   The computer system of claim 7, wherein the bus bridge is a south bridge.

1   9.   The computer system of claim 7, wherein the wake-up signal is a power management event

2   (PME#) signal, and wherein the controller isolates the PME# signal from the bus bridge if the

3   PME# signal is low following a predetermined delay after a Power Good signal is de-asserted.

1   10.   The computer system of claim 9, further comprising:

2   a signal gate that couples the wake-up signal to the bus bridge, wherein the signal gate is

3   set to a "pass" state by the controller if the PME# signal is high following after a

4   predetermined delay following the de-assertion of the Power Good signal, and

5   wherein the signal gate is set by the controller to a "no-pass" state otherwise.

1   11.   A method for handling non-compliant devices in a computer, wherein the method

2   comprises:

3   detecting a transition of the computer to a reduced-power state;

4   pausing for a predetermined delay;

5   sampling one or more wake-up signals from one or more devices;

6   establishing a signal block against any asserted wake-up signals.

1   12.   The method of claim 11, further comprising:

2   removing any signal blocks against sampled wake-up signals that are de-asserted.

1   13.   The method of claim 11, wherein said detecting includes:

2   monitoring a Power Good signal; and

3   sensing a transition of the Power Good signal from an asserted state to a de-asserted state.

1   14.   The method of claim 11, wherein the one or more wake-up signals are power management

2   event (PME#) signals from devices resident on a peripheral component interconnect (PCI) bus.

1   15.   The method of claim 11, wherein the establishing includes:

2   setting a signal gate to isolate the asserted wake-up signals from a bus bridge.

1   16.   A computer system that comprises:

2   an expansion bus that includes a plurality of expansion bus signals;

3   a bus bridge coupled to the expansion bus; and

4   a controller coupled to receive at least one of the expansion bus signals and configured to

5   provide a gated signal to the bus bridge, wherein the gate signal is asserted only if

6   an received expansion bus signal is asserted and not blocked.

1   17.   The computer system of claim 16, wherein the controller determines whether the received

2   signals are driven in a non-standard manner, and wherein the controller blocks any received

3   expansion bus signals that the controller determines are driven in a non-standard manner.

1   18.   The computer system of claim 16, wherein the received expansion bus signals are wake-up

2   signals.

1   19.   The computer system of claim 16, wherein the receive expansion bus signals are power

2   management event (PME#) signals, and wherein said controller determines that a PME# signal is

3   driven in a non-standard manner if the PME# signal is determined to be low at a predetermined

4   time delay after a Power Good signal goes low.

1   20.   The computer system of claim 16, wherein the controller is a power management

2   controller.